AMENDMENTS TO THE CLAIMS:

1. (Currently Amended) An electrically conductive layer, comprising:

a copper alloy interconnection layer which fills a trench groove and includes a copper alloy comprising at least one of Ag, As, ~~P, Si,~~ Bi, and Sb~~, and Ti~~ at not less than 0.1 percent by weight, so as to increase a crystal grain size and reduce crystal grain boundaries,

wherein said copper alloy further includes at least one of Mo, Ta and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight, and

wherein said at least one of Mo, Ta and W being higher in density than copper is present on said crystal grain boundaries, whereby said at least one of Mo, Ta and W suppresses a diffusion of copper.

2. (Currently Amended) The electrically conductive layer as claimed in claim 1, wherein said at least one of Ag, As, Bi, ~~P,~~ and Sb~~, Si, and Ti~~ is included in said copper alloy in a range of not less than 0.1 percent by weight to not more than a maximum solubility limit to copper, so that said copper alloy is in a solid solution.

3. (Canceled)

4. (Original) The electrically conductive layer as claimed in claim 2, wherein said copper alloy further includes at least one of Cr and Ni in a range of not less than 0.1 percent by weight to not

more than 1 percent by weight.

5. (Canceled)

6. (Previously Presented) The electrically conductive layer as claimed in claim 2, wherein said copper alloy further includes at least one of Ge and Mg in a range of not less than 0.1 percent by weight to not more than a maximum solubility limit of copper.

7. (Canceled)

8. (Original) The electrically conductive layer as claimed in claim 6, wherein said copper alloy further includes at least one of Cr and Ni in range of not less than 0.1 percent by weight to not more than 1 percent by weight.

9-10. (Canceled)

11. (Currently Amended) The electrically conductive layer as claimed in claim ~~10~~ 1, wherein said interconnection layer exists on a barrier metal layer extending on a bottom and side walls of said groove.

12. (Currently Amended) An electrically conductive layer, comprising:

a copper alloy interconnection layer which fills a trench groove and includes a copper alloy comprising at least one of Mo, Ta and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight,

wherein the mass-transfer of copper is suppressed through said copper alloy,

wherein said copper alloy further includes at least one of Ag, As, ~~P, Si,~~ Bi, and Sb~~, and Ti~~ in a range of not less than 0.1 percent by weight to not more than a maximum solubility limit of copper, so as to increase a crystal grain size and reduce crystal grain boundaries,

wherein said copper alloy further includes at least one of Ge and Mg in a range of not less than 0.1 percent by weight to not more than a maximum solubility limit of copper, and

wherein said at least one of Mo, Ta and W being higher in density than copper is present on said crystal grain boundaries, whereby said at least one of Mo, Ta and W suppresses a diffusion of copper.

13-14 (Canceled)

15. (Canceled)

16. (Original) The electrically conductive layer as claimed in claim 12, wherein said copper alloy further includes at least one of Cr and Ni in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

17-19 (Canceled)

20. (Currently Amended) The ~~interconnection~~ electrically conductive layer as claimed in claim 12, wherein ~~said electrically conductive layer comprises~~ said copper alloy interconnection layer ~~within a~~ fills said trench groove, which is formed in an insulation layer.

21. (Currently Amended) The ~~interconnection~~ electrically conductive layer as claimed in claim ~~12~~ 20, ~~wherein said interconnection layer exists on~~ further comprising:

a barrier metal layer extending on a bottom and side walls of said trench groove, said copper alloy interconnection layer being formed on said barrier metal layer.

22. (Currently Amended) A semiconductor device, comprising:

a semiconductor substrate;

an insulation layer over said semiconductor substrate, and said insulation layer having a trench groove;

a barrier metal layer on a bottom and side walls of said trench groove; and

an interconnection layer formed on said barrier metal layer, and ~~said interconnection layer filling said trench groove,~~

~~wherein said interconnection layer comprises~~ comprising a copper alloy which fills said trench groove and includes at least one of Ag, As~~, P, Si~~, Bi, and Sb~~, and Ti~~ in a range of not less than 0.1 percent by weight to not more than a maximum solubility limit of copper, so that said

copper alloy is in a solid solution, so as to increase a crystal grain size and reduce crystal grain boundaries,

wherein said copper alloy includes at least one of Mo, Ta and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight, and

wherein said at least one of Mo, Ta and W being higher in density than copper is present on said crystal grain boundaries, whereby said at least one of Mo, Ta and W suppresses a diffusion of copper.

23. (Canceled)

24. (Original) The semiconductor device as claimed in claim 22, wherein said copper alloy further includes at least one of Cr and Ni in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

25-29 (Canceled)

30. (Currently Amended) A semiconductor device, comprising:

a semiconductor substrate;

an insulation layer over said semiconductor substrate, and said insulation layer having a groove;

a barrier metal layer on a bottom and side walls of said groove; and

an interconnection layer formed on said barrier metal layer~~, and said interconnection layer filling said groove,~~

~~wherein said interconnection layer comprises~~ and comprising a copper alloy which fills said groove and includes at least one of Mo, Ta and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight,

wherein said copper alloy further includes at least one of Ag, As, Bi, ~~P,~~ and Sb~~, Si and Ti~~ in a range of not less than 0.1 percent by weight to not more than a maximum solubility limit of copper, so that said copper alloy is in a solid solution, so as to increase a crystal grain size and reduce crystal grain boundaries, and

wherein said at least one of Mo, Ta and W being higher in density than copper is present on said crystal grain boundaries, whereby said at least one of Mo, Ta and W suppresses a diffusion of copper.

31. (Canceled)

32. (Previously Presented) The semiconductor device as claimed in claim 30, wherein said copper alloy further includes at least one Ge and Mg in a range of not less than 0.1 percent by weigh to not more than a maximum solubility limit of copper.

33. (Canceled)

34. (Original) The semiconductor device as claimed in claim 30, wherein said copper alloy further includes at least one of Cr and Ni in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

35-64 (Canceled)

65. (New) The electrically conductive layer according to claim 1, wherein said crystal grain boundaries exist along a longitudinal direction of said interconnection layer.

66. (New) The electrically conductive layer according to claim 1, wherein said copper alloy interconnection layer comprises a top surface leveled to a top surface of an insulation layer.

67. (New) The electrically conductive layer according to claim 12, wherein said copper alloy interconnection layer comprises a top surface leveled to a top surface of an insulation layer.

68. (New) The semiconductor device according to claim 22, wherein said interconnection layer comprises a top surface leveled to a top surface of said insulation layer.

69. (New) The semiconductor device according to claim 30, wherein said interconnection layer comprises a top surface leveled to a top surface of said insulation layer.

70. (New) The semiconductor device according to claim 30, wherein said interconnection layer is situated within said trench groove.

71. (New) An electrically conductive layer, comprising:

a copper alloy interconnection layer which fills a trench groove and includes a copper alloy comprising at least one of As, Bi, and Sb at not less than 0.1 percent by weight, so as to increase a crystal grain size and reduce crystal grain boundaries,

wherein said copper alloy further includes at least one of Mo, Ta and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight, and

wherein said at least one of Mo, Ta and W being higher in density than copper is present on said crystal grain boundaries, whereby said at least one of Mo, Ta and W suppresses a diffusion of copper.

72. (New) An electrically conductive layer, comprising:

a copper alloy interconnection layer which fills a trench groove and includes a copper alloy comprising at least one of Bi and Sb at not less than 0.1 percent by weight, so as to increase a crystal grain size and reduce crystal grain boundaries,

wherein said copper alloy further includes at least one of Mo, Ta and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight, and

wherein said at least one of Mo, Ta and W being higher in density than copper is present on said crystal grain boundaries, whereby said at least one of Mo, Ta and W suppresses a

diffusion of copper.

73. (New) An electrically conductive layer, comprising:

a copper alloy interconnection layer which fills a trench groove and includes a copper alloy comprising Bi at not less than 0.1 percent by weight, so as to increase a crystal grain size and reduce crystal grain boundaries,

wherein said copper alloy further includes at least one of Mo, Ta and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight, and

wherein said at least one of Mo, Ta and W being higher in density than copper is present on said crystal grain boundaries, whereby said at least one of Mo, Ta and W suppresses a diffusion of copper.